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TRANSMITTAL FORM

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First Named Inventor	Luo, Wenzhe
Art Unit	2819
Examiner Name	Peguy JeanPierre
Attorney Docket Number	021653-004300US

ENCLOSURES *(Check all that apply)*

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  - ☐ Fee Attached
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  - •Communication - Comments on Statement of Reasons for Allowance

Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Daniel Mao		
Date	February 13, 2006	Reg. No.	51,995

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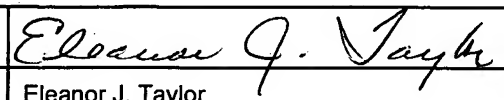
Signature			
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PATENT
Docket No.: 021653-004300US
Client Ref. No.: I-03-012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Wenzhe Luo et al.

Application No.: 10/808,721

Filed: March 24, 2004

For: DEVICE AND METHOD FOR LOW NON-LINEARITY ANALOG-TO-DIGITAL CONVERTER

Customer No.: 20350

Confirmation No.: 5625

Examiner: Peguy JeanPierre

Art Unit: 2819

COMMUNICATION - COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

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Sir:

In response to the Examiner's Statement of Reasons for Allowance, Applicant notes that claim 1 recites:

1. An apparatus for converting an analog signal to a digital signal, the apparatus comprising:

a plurality of capacitors including at least a first capacitor, a second capacitor and a third capacitor, a first capacitor associated with a first capacitance, a second capacitor associated with a second capacitance, a third capacitor associated with a third capacitance, the first capacitance being substantially equal to the second capacitance, the second capacitance being substantially equal to the third capacitance;

a plurality of resistors including at least a first resistor and a second resistor, the first resistor associated with a first resistance, a second resistor associated with a second resistance, the first resistance being substantially equal to the second resistance;

an operational amplifier including at least a first input terminal, a second input terminal and an output terminal;

wherein the first capacitor includes a first capacitor terminal and a second capacitor terminal, the second capacitor includes a third capacitor terminal and a fourth capacitor terminal, the third capacitor includes a fifth capacitor terminal and a sixth capacitor terminal, and the first capacitor terminal, the third capacitor terminal, and the fifth capacitor terminal are coupled to the first input terminal;

wherein the second input terminal is coupled to a first voltage;

wherein each of the second capacitor terminal, the fourth capacitor terminal, and the sixth capacitor terminal is capable of being coupled to anyone of the first voltage, an analog voltage, a second voltage, and a third voltage, the analog voltage associated with the analog signal;

wherein the first resistor includes a first resistor terminal and a second resistor terminal, the second resistor includes a third resistor terminal and a fourth resistor terminal, the first resistor terminal is coupled to the second voltage, the fourth resistor terminal is coupled to the first voltage, the first resistor and the second resistor being in series;

wherein the plurality of resistors corresponds to a plurality of resistor terminals, each of the plurality of resistors including two of the plurality of resistor terminals;

wherein the third voltage is provided by opening or closing a plurality of switches, each of the plurality of switches directly coupled to one of the plurality of resistor terminals;

wherein the apparatus is configured to convert the analog signal to the digital signal and is associated with a process related to a successive approximation register;

wherein the process includes processing information associated with the analog voltage and a fourth voltage; adjusting the fourth voltage in response to information associated

with the analog voltage and the fourth voltage, and determining the digital signal based on at least information associated with the fourth voltage;

wherein the fourth voltage is associated with at least a first voltage level of the second capacitor terminal, a second voltage level of the fourth capacitor terminal and a third voltage level of the sixth capacitor terminal, the first voltage level, the second voltage level and the third voltage level each being selected from a group consisting of the first voltage, the second voltage and the third voltage.

Applicant also notes that claim 3 recites:

3. An apparatus for converting an analog signal to a digital signal, the apparatus comprising:

a plurality of capacitors including at least a first capacitor and a second capacitor, a first capacitor associated with a first capacitance, a second capacitor associated with a second capacitance, the first capacitance being substantially equal to the second capacitance;

a plurality of resistors including at least a first resistor and a second resistor, the first resistor associated with a first resistance, a second resistor associated with a second resistance, the first resistance being substantially equal to the second resistance;

an operational amplifier including at least a first input terminal, a second input terminal and an output terminal;

wherein the first capacitor includes a first capacitor terminal and a second capacitor terminal, the second capacitor includes a third capacitor terminal and a fourth capacitor terminal, and the first capacitor terminal and the third capacitor terminal are coupled to the first input terminal;

wherein the second input terminal is coupled to a first voltage;

wherein each of the second capacitor terminal and the fourth capacitor terminal is capable of being coupled to anyone of the first voltage, an analog voltage, a second voltage, and a third voltage, the analog voltage associated with the analog signal;

wherein the first resistor includes a first resistor terminal and a second resistor terminal, the second resistor includes a third resistor terminal and a fourth resistor terminal, the

first resistor terminal is coupled to the second voltage, the fourth resistor terminal is coupled to the first voltage, the first resistor and the second resistor being in series;

wherein the plurality of resistors corresponds to a plurality of resistor terminals, each of the plurality of resistors including two of the plurality of resistor terminals;

wherein the third voltage is provided by opening or closing a plurality of switches, each of the plurality of switches directly coupled to one of the plurality of resistor terminals;

wherein the apparatus is configured to convert the analog signal to the digital signal and is associated with a process related to a successive approximation register;

wherein the process includes coupling the second capacitor terminal and the fourth capacitor terminal to the analog voltage, processing information associated with the analog voltage and a fourth voltage, adjusting the fourth voltage in response to information associated with the analog voltage and the fourth voltage, and determining the digital signal based on at least information associated with the fourth voltage;

wherein the fourth voltage is associated with at least a first voltage level of the second capacitor terminal and a second voltage level of the fourth capacitor terminal; the first voltage level and the second voltage level each being selected from a group consisting of the first voltage, the second voltage and the third voltage.

Applicant also notes that claim 13 recites:

13. A method for converting an analog signal to a digital signal, the method comprising:

providing an apparatus for converting the analog signal to the digital signal, the apparatus including:

a plurality of capacitors associated with a plurality of capacitances, each of the plurality of capacitances being substantially equal;

a plurality of resistors in series and associated with a plurality of resistances, each of the plurality of resistances being substantially equal;

wherein the plurality of capacitors is associated with a first plurality of capacitor terminals and a second plurality of capacitor terminals, the first plurality of capacitor terminals is coupled to each other, each of the second plurality of capacitor terminals is capable of being coupled to anyone of a first voltage, an analog voltage, a second voltage, and a third voltage, the analog voltage associated with the analog signal;

wherein the plurality of resistors is associated with a plurality of resistor terminals, a first terminal of the plurality of resistor terminals is coupled to the second voltage, a second terminal of the plurality of resistor terminals is coupled to the first voltage, each of the plurality of resistors including two of the plurality of resistor terminals;

wherein the third voltage is provided by opening or closing a plurality of switches, each of the plurality of switches directly coupled to one of the plurality of resistor terminals;

coupling each of the second plurality of capacitor terminals to the analog voltage;

decoupling each of the second plurality of capacitor terminals from the analog voltage;

coupling each of the second plurality of capacitor terminals to one selected from a group consisting of the first voltage, the second voltage, and the third voltage, the second plurality of capacitor terminals associated with a plurality of capacitor voltage levels respectively;

processing information associated with the analog voltage and a fourth voltage, the fourth voltage associated with the plurality of capacitor voltage levels;

adjusting the fourth voltage in response to information associated with the analog voltage and the fourth voltage;

determining the digital signal based on at least information associated with the fourth voltage.

None of the prior art references teach or suggest an apparatus or a method as recited in any of these claims.

Respectfully submitted,

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